Conciencia Digital

ISSN: 2600-5859
Vol. 7 No. 1.3, pp.172–184, March 2024

www.concienciadigital.org

La influencia del aprendizaje automático en el futuro del análisis de tiempo estático

*The influence of machine learning on the future of static time analysis*Julio Julio Torres Tello.

[1] Julio Torres Tello
Independent Researcher, Saskatoon, Canada.
Julytorrest@gmail.com

https://orcid.org/0000-0001-9694-6578

Scientific and Technological Research Article
Sent: 12/15/2023
Revised: 18/01/2024
Accepted: 10/02/2024
Published:22/03/2024
DOI:**https://doi.org/10.33262/concienciadigital.v7i1.3.2964**

Please quote: Torres Tello, J. (2024). The influence of machine learning on the future of static timing analysis. ConcienciaDigital, 7(1.3), 172-184.https://doi.org/10.33262/concienciadigital.v7i1.3.2964

DIGITAL CONSCIOUSNESS,andIt is a multidisciplinary, quarterly journal, which will be published electronically. Its mission is to contribute to the training of competent professionals with a humanistic and critical vision who are capable of presenting their research and scientific results to the same extent that their intervention promotes positive changes in society.https://concienciadigital.org
The journal is published by Editorial Ciencia Digital (a prestigious publisher registered with the Ecuadorian Book Chamber with membership number 663).www.celibro.org.ec

Conciencia Digital

ISSN: 2600-5859
Vol. 7 No. 1.3, pp.172–184, March 2024

www.concienciadigital.org

Palabras claves:
Aprendizaje automático, Análisis de tiempo estático, Caracterización, Automatización del diseño electrónico, Semiconductores

Resumen

Introducción. El Análisis de Tiempo Estático (ATS), fundamental en el diseño de circuitos integrados, implica evaluar el rendimiento temporal de circuitos digitales bajo diversas condiciones para cumplir ciertas restricciones, mediante simulación. A pesar de su importancia, el ATS tradicional enfrenta varias limitaciones a la hora de considerar en sus modelos la creciente complejidad del proceso de fabricación de circuitos integrados. La inclusión de Inteligencia Artificial (IA) se vislumbra como una solución prometedora para mejorar la precisión y eficiencia del ATS, reduciendo así los ciclos de diseño en la industria electrónica. **Objetivo.** Estudiar la influencia que tiene en la actualidad, y que puede tener a futuro la inclusión de la IA para la optimización del ATS, y por lo tanto para reducir los ciclos de diseño en la industria de la electrónica. **Metodología.** La IA se ha integrado en el Análisis de Tiempo Estático (ATS), mejorando la precisión y eficiencia al estimar retrasos, modelar variaciones de proceso y optimizar rutas y procesos de síntesis. Esta integración permite abordar la complejidad y variabilidad de los circuitos integrados modernos, acelerando la convergencia del diseño, reduciendo iteraciones y mejorando la calidad del diseño. Además, IA se aplica en la caracterización del modelo para ATS, utilizando simulaciones adaptativas para acelerar el proceso de verificación y reducir significativamente el tiempo de comercialización, crucial en la industria de semiconductores. En este artículo se hace una revisión del estado actual y las proyecciones a futuro del aporte de la IA en el ATS. **Discusión.** El futuro del ATS promete una serie de avances que buscan mejorar sus capacidades y abordar los desafíos emergentes en el diseño de circuitos integrados. Estos desarrollos incluyen una mayor integración con el Aprendizaje Automático (ML) para mejorar la precisión y eficiencia. Con la evolución hacia nodos de proceso más pequeños, el ATS deberá adaptarse para manejar la mayor complejidad y variabilidad introducida, posiblemente empleando algoritmos de ML más sofisticados. Además, se espera que el ATS se enfoque más en consideraciones de potencia y confiabilidad, incorporando métricas adicionales y análisis de datos más complejos, posiblemente con la ayuda de la IA, para garantizar la eficiencia energética y la robustez contra problemas de confiabilidad. **Conclusión.** El futuro del ATS se perfila hacia

ISSN: 2600-5859
Vol. 7 No. 1.3, pp.172–184, March 2024

una constante innovación y adaptación para satisfacer las cambiantes necesidades de la industria de semiconductores. Aprovechando avances tecnológicos y metodológicos, el ATS jugará un papel crucial en asegurar la entrega puntual de diseños de circuitos integrados de alto rendimiento y fiabilidad. Dada la capacidad de optimización y análisis de datos de la IA, su potencial revolucionario en el ATS es considerable, especialmente ante la creciente inclusión de requisitos cada vez más exigentes. **Área de la ciencia:** ingeniería electrónica.

Keywords:
Machine learning, Static timing analysis, Characterization, Electronic design automation, Semiconductors

Abstract

Introduction. Static Timing Analysis (STA), fundamental in the design of integrated circuits, involves evaluating the temporal performance of digital circuits under various conditions to meet certain constraints, through simulation. Despite its importance, traditional ATS faces several limitations when considering the increasing complexity of the integrated circuit manufacturing process in its models. The inclusion of Artificial Intelligence (AI) is seen as a promising solution to improve the precision and efficiency of the ATS, thus reducing design cycles in the electronics industry. objective. To study the influence that the inclusion of AI has, and may have in the future, for the optimization of the ATS, and therefore to reduce design cycles in the electronics industry. Methodology. AI has been integrated into Static Time Analysis (STA), improving accuracy and efficiency when estimating delays, modeling process variations, and optimizing routes and synthesis processes. This integration addresses the complexity and variability of modern integrated circuits, accelerating design convergence, reducing iterations, and improving design quality. Additionally, AI is applied in model characterization for ATS, using adaptive simulations to accelerate the verification process and significantly reduce time to market, crucial in the semiconductor industry. This article reviews the current state and future projections of the contribution of AI in the ATS. Discussion. The future of STA promises a series of advances that seek to improve its capabilities and address emerging challenges in integrated circuit design. These developments include greater integration with Machine Learning (ML) to improve accuracy and efficiency. With the evolution towards smaller process nodes, STA will need to adapt to manage the

ISSN: 2600-5859
Vol. 7 No. 1.3, pp.172–184, March 2024

increased complexity and variability introduced, employing more sophisticated ML algorithms. Additionally, STA is expected to focus more on power and reliability considerations, incorporating additional metrics and more complex data analysis, with the help of AI, to ensure energy efficiency and robustness against reliability issues. Conclusion. The future of ATS is shaping up to be constant innovation and adaptation to meet the changing needs of the semiconductor industry. Technological and methodological advances will play a crucial role in ensuring the timely delivery of high-performance and reliable integrated circuit designs. Given AI's data analysis and optimization capabilities, its revolutionary potential in ATS is considerable, especially with the growing inclusion of increasingly demanding requirements.

Introduction

Static Timing Analysis (STA) is a crucial step in the integrated circuit (IC) design process within the field of electronic design automation (EDA). It involves evaluating the timing performance of a digital circuit under various conditions to ensure that it meets certain constraints. The primary goal of STA is to determine whether the circuit operates correctly with respect to timing requirements such as settling time, hold time, clock-to-output delay, and maximum operating frequency. These constraints are critical for proper operation of digital circuits and must be met to avoid problems such as settling and hold violations, which can lead to incorrect or unreliable circuit operation (Blaauw et al., 2008; Forzan & Pandini, 2009).

ATS works by simulating circuit behavior using mathematical models to predict signal propagation delays through various paths within the design. This analysis considers factors such as delays introduced by gates, interconnect delays, clock signal variations, and environmental variations to accurately assess the timing performance of the circuit (Muthukrishnan & Sathasivam, 2022).

The process that follows this analysis typically involves the following steps (Kaeslin, 2015): (1) Netlist Generation: The circuit design is represented as a netlist, which is a description of the interconnections between the various components (such as gates, flip-flops, and interconnects) in the circuit. (2) Constraint Definition: Timing constraints are specified by the designer based on the requirements of the design and the target technology. These constraints include parameters such as clock frequencies, input arrival times, required output times, and maximum delay paths. (3) Timing Analysis: The timing

analyzer calculates the arrival times and required timings of signals at different points in the circuit, considering the effects of logic gates, interconnects, and clock signals. It identifies critical paths and verifies whether they comply with the specified timing constraints. (4) Constraint Verification: The results of the timing analysis are compared to the specified timing constraints to identify potential violations. If violations are found, the designer may need to revise the design or adjust constraints to achieve temporal closure. (5) Optimization: Techniques such as buffer insertion, clock tree synthesis, and gate sizing can be applied to optimize the timing performance of the circuit and eliminate timing violations.

This analysis is essential to ensure reliable operation of digital circuits and plays a vital role in the overall integrated circuit design process. It allows designers to identify and address temporary problems early in the design cycle, reducing the risk of costly errors and ensuring that the final product meets performance requirements (Design & Reuse, sf).

The ATS has been instrumental in VLSI chip design since the 1990s, serving as a crucial tool for timing verification and facilitating timing optimization. Despite its advantages such as linear run-time scalability and conservative delay estimation, traditional Deterministic ATS (DSTA) faces limitations in accurately modeling process variations, especially intra-die variations, which have become significant with advancing process scaling. This inadequacy leads to challenges in estimating circuit delays effectively. Static Statistical Timing Analysis (SSTA) emerges as a solution, aiming to address the shortcomings of DSTA by providing more accurate and efficient methods for modeling process variations. Recent years have seen a surge in research focused on SSTA, highlighting its importance in overcoming the limitations of DSTA and improving the accuracy of timing analysis in modern IC design (Blaauw et al., 2008; Forzan & Pandini, 2009).

As new silicon technologies continue to shrink transistor size, it becomes increasingly difficult to precisely control process parameters during manufacturing. As a consequence, both the number and magnitude of independent sources of variations are increasing. These unavoidable fluctuations in process parameters can significantly impact design performance, often resulting in a considerable loss of parametric performance (Forzan & Pandini, 2009).

On the other hand, new models based on Artificial Intelligence (AI) have been successfully applied in many fields, such as medicine (Chae et al., 2020; Jiang et al., 2018), transportation (Castro-Zunti et al., 2020) and security (Torres-Tello et al., 2020), mainly because they can effectively discover complex structures in large data sets (Han et al., 2019). The EDA industry can also benefit from this technology.

ISSN: 2600-5859
Vol. 7 No. 1.3, pp.172–184, March 2024

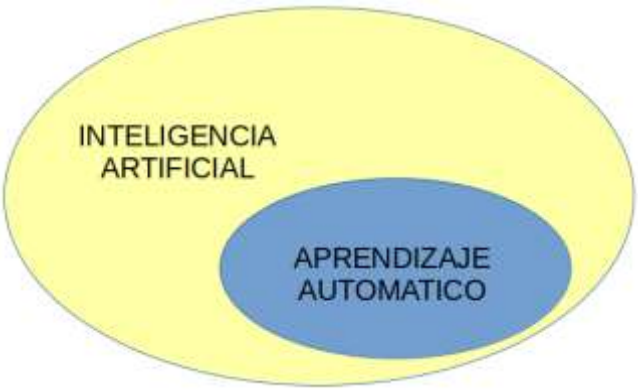
This article studies the influence that the inclusion of AI has today, and may have in the future, for ATS optimization, and therefore for reducing design cycles in the electronics industry.

Methodology

AI is a concept as old as computers themselves, and saw its first real breakthroughs in the mid-20th century (Chollet, 2017; Raschka, 2015), when some scientists attempted to mathematically and electronically replicate the basic understanding that was available at the time about how neurons in the human brain work. However, in its early days, the most successful AI approaches consisted of what is called symbolic AI, or the idea that intelligence could be achieved by programming a sufficiently large set of rules. This approach lacked flexibility and has now been almost entirely replaced by machine learning (ML), a subfield of AI (Figure 1), which uses learning algorithms to extract information from data in order to make predictions, rather than humans trying to derive complicated rules (Raschka, 2015).

Figure 1

Machine learning, or machine learning, as part of artificial intelligence



There are many definitions of ML in the literature, however, they all agree on the basic idea that machines can learn from data (Chollet, 2017; Géron, 2019; Goodfellow et al., 2016; Raschka, 2015). Some also point out that it is primarily an engineering problem (Géron, 2019), due to its statistical foundations, its heavy reliance on computers, and its relaxed confidence intervals (Goodfellow et al., 2016). This highly application-oriented nature makes it a science, but also an art (Géron, 2019; Raschka, 2015). All of this has some implications; The most important one is a paradigm shift in programming, which is best visualized in Figure 2. In classical programming, a human has to write a set of rules that operate on data to provide some answers, whereas, with ML, a computer uses the data and known answers to derive a set of rules that can then operate on new data to generate original answers (Chollet, 2017). This process, of course, still requires humans

ISSN: 2600-5859
Vol. 7 No. 1.3, pp.172–184, March 2024

to write a program. The main change is that programmers now do not need to hard code the rules, but rather need to specify a limited model space within which the computer needs to find an optimal model that fits the data, with the help of a feedback signal (Chollet, 2017). This process is called training.

Figure 2

Machine learning, a new programming paradigm

Machine learning has been increasingly integrated into ATS to improve its accuracy, efficiency, and scalability. ML algorithms are used for several purposes within ATS, including delay estimation, statistical timing analysis (SSTA), path identification and optimization, clock tree synthesis, and timing violation prediction and correction.

ML techniques enable more accurate prediction of delay values in digital circuits by learning from vast amounts of data, providing more precise estimates compared to traditional analytical methods. In SSTA, ML models are trained to model process variations and other sources of uncertainty, enabling a more complete understanding of circuit performance under varying conditions. ML algorithms are also employed to identify critical timing paths in complex designs more efficiently, prioritize paths for optimization, and optimize clock tree synthesis processes by predicting clock skew and variation, minimizing clock distribution delays and reducing power consumption. Furthermore, ML can predict potential timing violations early in the design cycle and recommend corrective actions to mitigate these violations, thereby improving timing closure and overall design quality.

Overall, integrating machine learning into static timing analysis enables designers to address the increasing complexity and variability of modern integrated circuits more effectively, leading to faster design convergence, reduced design iterations, and improved overall design quality.

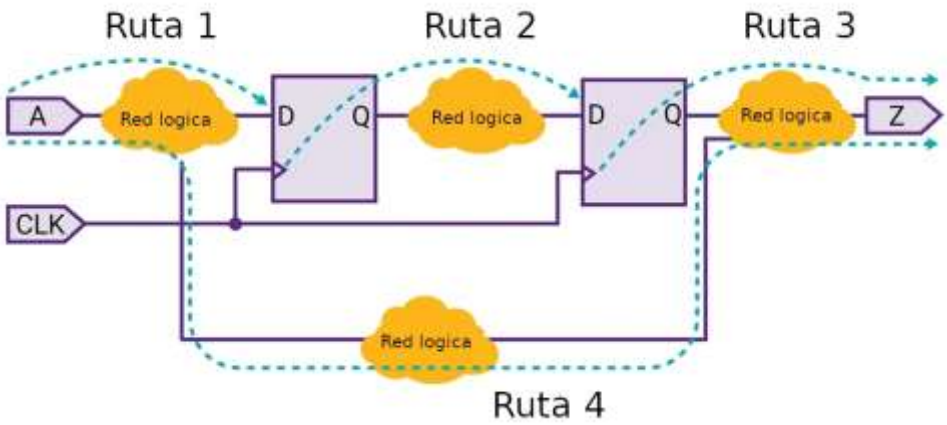
Conciencia Digital
ISSN: 2600-5859
Vol. 7 No. 1.3, pp.172–184, March 2024
www.concienciadigital.org

To ensure the optimal performance of new semiconductor designs or processes, it is crucial to verify all components from the most basic blocks to custom circuits through simulations, considering variables such as operating voltage and temperature and local device variations. However, this task is enormously demanding, especially to achieve rigorous verification standards such as those demanded by current technology, which requires a massive amount of samples to obtain results with high statistical confidence. Model characterization for ATS also involves a large number of simulations, necessary for timing, power and area analysis in digital designs. Innovations have now emerged that use ML to accelerate this process (Tan & Santarini, 2023), while maintaining production accuracy. This technology uses adaptive simulations to obtain initial results, intelligently selects sample points and adjusts the results to obtain accurate measurements, allowing production results to be achieved at a significantly faster speed than traditional methods. This technology allows design teams to significantly reduce time to market.

Figure 3 shows an example of the different paths that an electronic signal can take within a circuit. Given the complexity of current designs, it is practically impossible to consider all paths at the same time, especially when considering variations in both manufacturing processes and operating conditions. Without the help of ML tools, the results of these analyses would lack reliability, and given the increasing complexity, there is an urgent need to find tools that involve even more holistic approaches and are able to further optimize simulations and error control.

Figure 3

Critical timing paths. Each logic network represents a combinational logic network, which introduces its own delay different from the others.



Fountain: Synopsys (sf)

Discussion

The future of ATS offers several possible developments that are expected to enhance its capabilities and address emerging challenges in integrated circuit (IC) design. Some key aspects of the future of ATS include:

Greater integration with machine learning: ATS is likely to continue to integrate machine learning techniques to improve accuracy and efficiency. ML algorithms can help better model process variations, optimize time paths, and predict time violations, ultimately leading to faster design closure and improved quality of results.

Advanced Processing Nodes: As semiconductor technology advances toward smaller process nodes, ATS will need to adapt to handle the increased complexity and variability introduced by factors such as process variations and interconnect effects. Future ATS tools should focus on developing more sophisticated models and algorithms, such as ML, for example, to analyze timing at these advanced process nodes.

Time for emerging technologies: As new technologies such as silicon photonics, 3D integration, and quantum computing become more common, ATS will need to evolve to support timing analysis for these emerging technologies. This may involve developing new models and methodologies tailored to the unique characteristics of these technologies.

*Interdisciplinary collaboration:*ATS will increasingly involve collaboration with other fields such as circuit design, physical design, and manufacturing. Closer integration between timing analysis and other stages of the design flow will enable more holistic optimization and better overall design quality. ML algorithms can be included throughout the design process, which in turn could achieve optimizations at different levels.

*Focus on power and reliability;*In addition to traditional timing metrics, future STA tools are likely to place more emphasis on power consumption and reliability considerations. This includes analyzing timing under different power modes, optimizing energy efficiency, and ensuring robustness against reliability issues such as aging and variability. This vast amount of data may be impossible to analyze without the help of AI.

Conclusions

- Overall, the future of ATS needs to be characterized by continued innovation and adaptation to meet the evolving needs of the semiconductor industry. By leveraging advances in technology and methodologies, ATS will play a vital role in ensuring the timely delivery of high-performance and reliable IC designs.
- In recent decades, AI has found applications in many areas, including electronic design. However, the specificity required in this case means that the development of AI tools in this application is still limited.

- Given the potential for optimization and data analysis that AI provides, it can have a revolutionary impact on ATS, especially considering the growing inclusion of increasingly demanding requirements.

Conflict of interest

The author declares that there is no conflict of interest in relation to the submitted article.

Bibliographic References

Blaauw, D., Chopra, K., Srivastava, A., & Scheffer, L. (2008). Statistical timing analysis: from basic principles to state of the art. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 27(4): 589–607.https://doi.org/10.1109/TCAD.2007.907047

Castro-Zunti, R.D., Yepez, J., & Ko, S.-B. (2020). License plate segmentation and recognition system using deep learning and OpenVINO. IET Intelligent Transport Systems, 14(2): 119–126. https://doi.org/10.1049/iet-its.2019.0481

Chae, KJ, Jin, GY, Ko, SB, Wang, Y., Zhang, H., Choi, EJ, & Choi, H. (2020). Deep learning for the classification of small (≤2 cm) pulmonary nodules on CT imaging: a preliminary study. Academic Radiology, 27(4), e55–e63. https://doi.org/10.1016/j.acra.2019.05.018

Chollet, F. (2017). Deep learning with python (1st edition). Manning Publications.

Design & Reuse. (sf). Integration of design-for-analysis in IC layout considerations to meet the challenges of shrinking technology. https://www.design-reuse.com/articles/18531/design-for-analysis-ic-layout.html

Forzan, C., & Pandini, D. (2009). Statistical static timing analysis: A survey. Integration, 42(3): 409–435. https://doi.org/10.1016/j.vlsi.2008.10.002

Géron, A. (2019). Hands-on machine learning with scikit-learn, Keras, and TensorFlow: concepts, tools, and techniques to build intelligent systems (2 edition). O'Reilly Media.

Goodfellow, I., Bengio, Y., & Courville, A. (2016). Deep Learning. The MIT Press.

Han, Z., Zhao, J., Leung, H., Ma, K.F., & Wang, W. (2019). A review of deep learning models for time series prediction. IEEE Sensors Journal, 21(6): 7833-7848.https://doi.org/10.1109/JSEN.2019.2923982

Jiang, Z., Zhang, H., Wang, Y., & Ko, S.-B. (2018). Retinal blood vessel segmentation using fully convolutional network with transfer learning. Computerized Medical

Imaging and Graphics, 68: 1–15. https://doi.org/10.1016/j.compmedimag.2018.04.005

Kaeslin, H. (Ed.). (2015). Chapter 4—Circuit modeling with hardware description languages. Top-Down Digital VLSI Design (pp. 179–300). Morgan Kaufmann. https://doi.org/10.1016/B978-0-12-800730-3.00004-6

Muthukrishnan, P., & Sathasivam, S. (2022). A technical survey on delay defects in nanoscale digital VLSI circuits. Applied Sciences, 12(18): 9103. https://doi.org/10.3390/app12189103

Raschka, S. (2015). Python Machine Learning, 1st Edition. Packt Publishing.

Tan, W.-L., & Santarini, M. (2023). How Siemens EDA's Solid achieved production-grade AI in EDA applications. Siemens Digital Industries Software. https://resources.sw.siemens.com/en-US/white-paper-how-siemens-edas-solido-achieved-production-grade-ai-in-eda-applications

Torres-Tello, J., Guamán, AV, & Ko, S.-B. (2020). Improving the detection of explosives in MOX chemical sensors array with LSTM Networks. IEEE Sensors Journal, 20(23): 14302–14309. https://doi.org/10.1109/JSEN.2020.3007431

Synopsys. (sf). What is Static Timing Analysis (STA)? –How STA works? https://www.synopsys.com/glossary/what-is-static-timing-analysis.html

Conciencia Digital

ISSN: 2600-5859
Vol. 7 No. 1.3, pp.172–184, March 2024

www.concienciadigital.org